

Delivering Power Integrity Solutions for Advanced IC Packages

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Introduction

As the push towards deep-submicron, system-in-chip and system-on-chip continues, the industry is moving toward higher pin-count, more complex, higher density packaging with increased functionality, operating frequency, lower operating voltages and reduced package size. The demand on electrical performance characterization of high-density, multi-layer and three dimensional chip configurations such as flip chip, BGA, and system-in-package becomes the difficult challenge faced by EDA companies.

Package power integrity is one of the key challenges due to the current surges caused by simultaneous switching. With the decrease in voltage supply, the sensitivity of ICs to the voltage fluctuation increases because the threshold voltage is scaled down. A good chip power delivery system has to maintain steady power and ground rails during core switching.

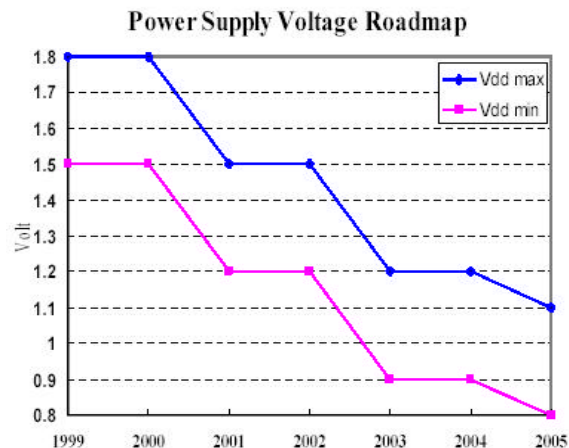


Figure 1. Power supply voltage roadmap: International Technology Roadmap for Semiconductors(ITRS)

Power integrity is measured by observing power and ground levels in the power delivery system during many cycles of on-die switching. The power delivery system is composed of the power and ground chip connections, power and ground vias, planes or strips for power and ground and lands or pins in the package substrate dedicated to power and ground. The voltage deviation is expected during switching due to the inductive effects of power delivery system parasitics or package parasitics.

When output drivers are switching simultaneously, the voltage fluctuation, which is referred to as simultaneous switching noise (SSN), is given by the formula $V = L (di/dt)$. The voltage deviation due to the di/dt switching is proportional to the power delivery network loop inductance, L . An I/O switching from high to low or low to high is discharging or charging the capacitor that loads the I/O, the resulting di/dt is cumulative and gets higher with increased simultaneous switching outputs. Therefore, the higher the di/dt , the higher is the

voltage fluctuation amplitude. Figure 2 demonstrates the simultaneous switching effects while 10 buffers are active simultaneously.

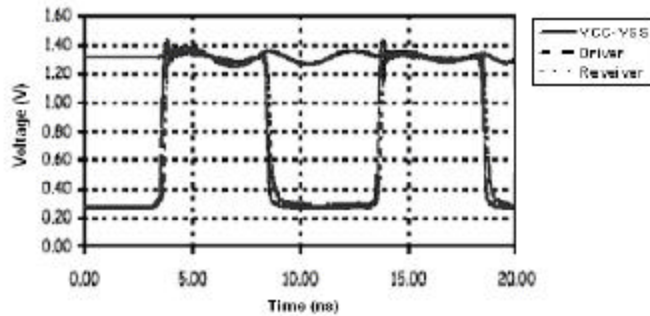


Figure 2. Illustration of SSN when 10 drivers are active

Package Power Integrity Analysis

The power delivery network loop inductance, however, changes with respect to each signal net. This is directly related to the proximity of VCC and VSS pins, planes, and vias to the I/O path, and to discontinuities in the return path. Therefore, a good package parasitic model is expected to have an accurate and complete consideration of the power distribution system and the package signal distribution network and the coupling between the two.

In ICEMAX 2.0, the user can perform a multi-level, multi-port analysis which characterizes the power delivery system precisely. ICEMAX uses an unstructured finite volume code to compute the field distribution and parasitics for the power delivery network. Figure 3 shows a typical mesh generated by ICEMAX for a VCC plane in a 4-layer BGA design.

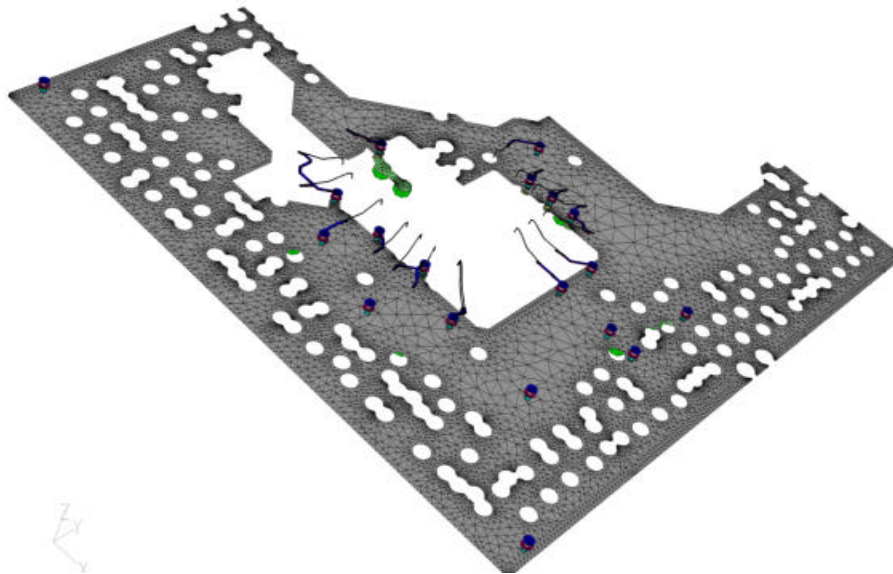


Figure 3. A typical mesh for a VCC net, generated by ICEMAX

For a complicated multi-port net such as the one shown in Figure 3, ICEMAX allows users to generate models with different levels of refinement. Performing the LEVEL 0 simulation, an effective lumped element model of the power/ground net will be given which represents the rough estimation of the total parasitics of the power/ground net regardless of the power/ground chip connections and power/ground pins. As a result, a one-input-one-output equivalent circuit will be reported.

A more accurate model can be extracted at LEVEL 1 or LEVEL 2. At LEVEL 1 simulation, when the ground/power pins or ground/power chip connections are falling into a very small part of the package, which can be simply treated as one pin or one connection, an equivalent multi-port network with respect to multi-pins/multi-connections will be given as a multi-input-one-output equivalent circuit or a one-input-multi-output equivalent circuit. At LEVEL 1 simulation, the coupling among PWR pins or GND pins, which are treated as one port, will not be fully captured. The LEVEL 2 simulation can be used whenever LEVEL 0 and LEVEL 1 simulation are not adequate to track the loop inductive effects, which gives the user the full multi-port results of the power/ground chip connections and VCC/GND pins. In this case, the coupling between the PWR pins and GND pins will be fully computed for the equivalent circuit model. The illustration of ICEMAX LEVEL 0, LEVEL 1, and LEVEL 2 simulations are shown in Figure 4(a), 4(b), and 4(c) respectively.

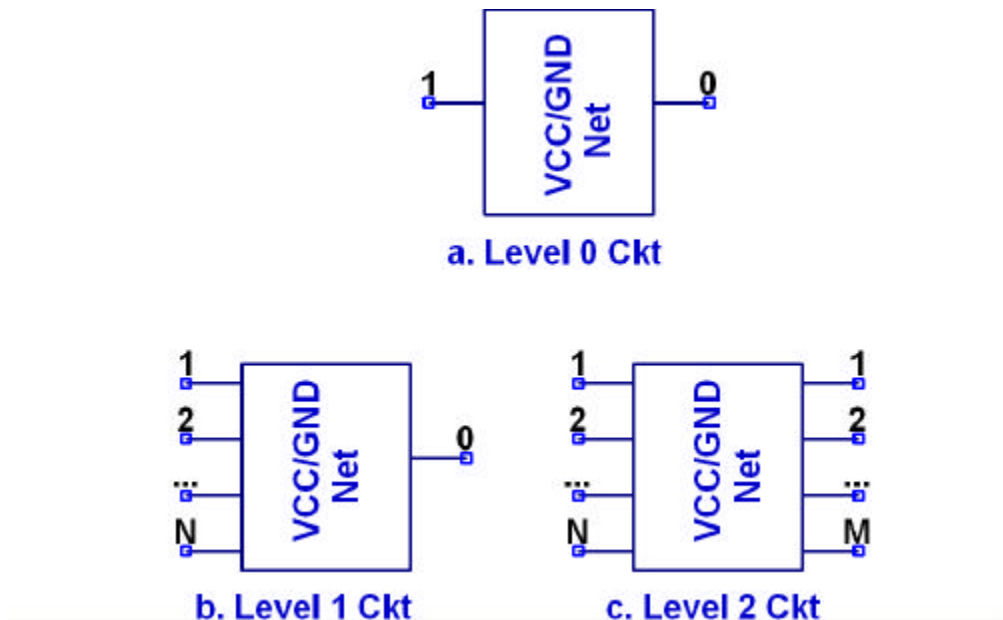


Figure 4. ICEMAX LEVEL 0, LEVEL 1, LEVEL 2 multi-port representation of VCC or GND nets

Using the parasitics generated from ICEMAX, the waveform along I/O trace taking care of the power/ground nets effects can be analyzed in a SPICE circuit simulator. Signal trace models and nonlinear transistor models are connected to the power/ground nets model, the voltage fluctuation due to the switching can be simulated as well as the timing push-out effects on the victim signal, as shown in Figure 5.

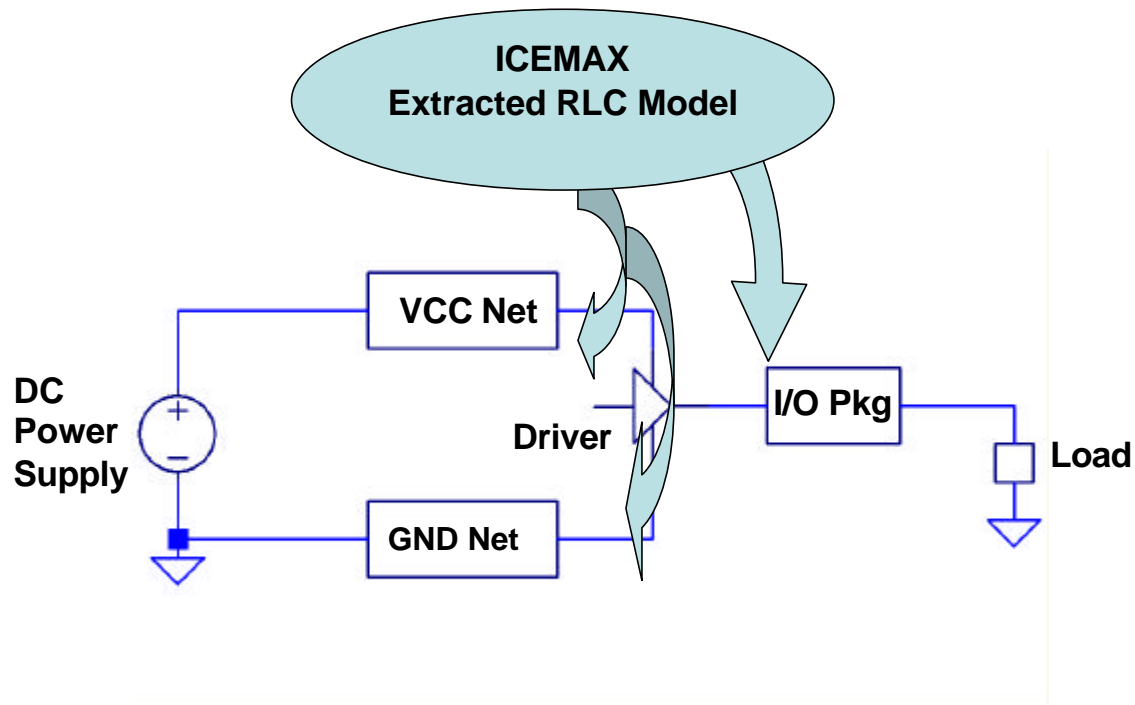


Figure 5. Simultaneous Switching Noise (SSN) simulation circuit

Summary

Power distribution system design is becoming an increasingly difficult challenge for IC designers. This article describes the package level power integrity analysis strategy with the use of 3D package characterization tool and SPICE circuit simulator. The use of ICEMAX, an advanced, fast chip package parasitic extraction tool, delivers the right solution for power integrity of many types of chip packages. ICEMAX uses finite volume-based numerical technology to solve for electromagnetic effects, combined with advanced memory optimization methodologies for fast and accurate RLC model extraction of package I/O nets and PWR/GND nets.